The 2004 China PCB Market and Technology:
A Brief Review

1. The China Market: a brief review

The Printed Circuit Board (PCB) industry reaped a bumper harvest in 2004. Revenues have been good, but a surplus in supply is one worry. Distributors say that, although the prices of raw materials and of PCBs have soared, market demand is still powerful, and there has been no impact on profits. Meanwhile, the PCB market keeps showing strong growth. What is worrying distributors is that a surplus in supply may lead to a price war this year.

In a situation in which the price of raw materials became flexible to some extent in the fourth quarter of 2004, the price of PCBs has not fallen; thus, the industry has not influenced the management approach of distributors during low seasons. As the price of PCBs stay at the same level in the fourth quarter to 2005, distributors contend that the PCB market will continue to have good prospects.

A spot market distributor introduces such products with steady markets as automobiles, high-frequency wireless devices, home appliances, and so forth, that are holding up the PCB industry. As the macro environment improves, the demand for these products has grown. In the fourth quarter of 2004, the PCB market adjusted and grew because of the high demand, and the phenomenon of shortages of supply still occurred often.

According to statistical data from Prismark, a tide of changes that takes place once every three years has already happened for 2004. Since the enterprises have been making profits and have been investing them in improving and expanding their operations and, at the same time, there has been continued growth in demand for broadband, it is expected that the servers will continue to grow steadily. As Taiwan and South Korea have been investing actively in expanding the market for TFT-LCD panels, after six generations of LCD factories open successively, the market for panels can be expected to grow gradually. As the demand for such products is still growing slowly but steadily, the total output value of PCBs can still grow by about 5-8% in 2005. However, because the PCB industry did extremely well in 2004, this will result in an increase in production. The question of a surplus of supply still hangs over the whole PCB industry. Given a flexible PCB regime, because 80% of applications come from the cellular phone industry and 10% from the TFT-LCD industry, the market generally estimates that the demand for LCDs will bottom out in the second quarter of 2005, that the demand for cellular phones will decrease in the first quarter, and that the demand for PCBs will bottom out in the first quarter of 2005. Correspondingly, there will be a surplus
of production and supply. In a situation of double-phase growth and decline, a price war is inevitable.

In 2005, PCB manufacturers may face the problem of oversupply, estimate at about 20%.

2. Technology: a brief review

Due to the trends of electronic miniaturization, ever-increasing transmission speeds, and environmental conservation, it has become absolutely necessary to test the reliability of dielectric materials, board designs and manufacturing processes, and high-density PCBs. In the following paragraph, an overview of the major PCB technologies in 2004 is presented. These technologies have been widely discussed in global magazines.

2.1 Advanced materials technology

2.1.1 High-speed materials for 3-6 GHz Design

High-speed circuit designs emphasize the usefulness of passive circuit elements. When designing circuits with speeds of below 1 GHz, passive elements such as the dielectric substrate can generally be ignored and standard FR-4 materials usually work very well. But as frequencies increase beyond 1 GHz, the passive circuit elements must be taken into account. Primary considerations for circuit design in the 3-6 GHz include the skin effect, surface roughness, the proximity effect, EMC, and dielectric properties. The two dielectric properties that primarily affect the design of high-speed circuits are the dielectric constant (Dk) and the dissipation factor (Dr). The percentage of resin, absorption of moisture, and the temperature, all of which affect the dielectric properties, should be considered when deciding which laminate is best for a high-frequency design.

![Figure 1](image1)  
Figure 1. Variation permittivity at different resin contents

![Figure 2](image2)  
Figure 2. Variations in Dk at different temperatures

(Source: PCD&M Magazine, Nov 04, Vol. 21, No. 11)
Figures 1 and 2 illustrate the variations in the dielectric constant at different resin contents and temperatures, respectively. There are many resin systems and other substrates available for applications in the 3-6 GHz range. However, the properties to be evaluated will be the same. Other factors such as the ease of processing and cost have to be considered.

2.1.2 Teflon Material - Through the activation of holes

Board designers now incorporate Teflon material in the design of voltage-controlled oscillators, IF amplifiers, ground spectrum devices, and other strip-line and micro-strip circuits. In addition, Teflon is now commonly specified as the required material for the fabrication of single, double, and even multilayer high-frequency PCBs. The wider use of Teflon material is due to its improved specifications, for instance, better electrical and mechanical stability by incorporating filler, a low CTE, a low dielectric constant, and low moisture absorption. However, its hydrophobic characteristics present manufacturing challenges as liquids bead and roll off their surface. As a result, Teflon material requires treatment after drilling for both single and double-sided panels. Unless panels are treated prior to metallization, there will be little success in covering the wall of a hole. The two most widely used methods of treating Teflon material are wet chemical processing with sodium etch (Na) and gas plasma processing using a combination of Hydrogen (H₂) and Nitrogen (N₂). The Na and plasma H₂/N₂ processes have yielded the best results.

2.1.3 Lead-free Hot Air Soldering

The European Union (EU) has strongly suggested that all electronics manufactured or sold in its jurisdiction be lead free by 2006, and Japan already has such a mandate in effect. In North America, it is estimated that the next largest source of lead contamination in run-off water from landfills after lead acid batteries is from discarded electronic devices. Lead-free solder alloys have been developed in many forms. The most promising of these have acceptable structural and conductive properties, sometimes exceeding that of eutectic solder, but usually requiring higher working temperatures and additional process steps to be used in a manufacturing environment.

The best replacement for tin-lead solder would be one that has a working range below 250°C and does not require exotic process changes to provide consistent results. Two of the leading candidates for this lead-free substitute seem to be alloys of eutectic tin-copper and tin-silver in combination with various trace metals and/or organics, with melting a temperature of approximately 227°C and 216°C, respectively.
2.2 Design and manufacture

2.2.1 High-speed design

The decrease in interconnect delays due to board size has not kept pace with the decreases from the shrinking die sizes and increased clock speeds prevalent in many components used today. As a result, board-level interconnect delays account for a much larger percentage of the overall timing budget, resulting in a dramatic decrease in the overall timing margins of designs.

Figure 3. Complete analysis of both digital timing (digital) and signal integrity (analog)

Figure 4. Small window of delay variation.

(Source: PCD&M Magazine, Dec 04, Vol. 21, No. 12)

Figure 3 illustrates the complete analysis of both digital timing and signal integrity. Designers often see only a small window of delay variation, as shown in Figure 4. In fact, there are a number of ways in which issues of timing can be resolved, including manual methods, timing waveform, static timing analysis, fully functional simulators, and clock path analysis. Today's timing analysis and verification tools effectively allow designers to find and eliminate timing problems in their designs. Incorporating accurate timing margins under extreme conditions and understanding specific timing sensitivities in the circuit ensures robust system operation. Eliminating timing problems early in the design cycle reduces, and may even eliminate, multiple design iterations and costly reworking.

2.2.2 High volume via-filling manufacturing

With a greater proportion of new board designs relying on through-vias and conductive-filled vias, the traditional manual and semiautomatic via-filling processes present PCB fabricators with a throughput bottleneck.

A repeatable, high-throughput via-filling technique is needed. This technology enables direct pressure to be applied vertically to the via-fill material. In addition to conductive epoxies, the via-fill materials currently in use include insulating polymers
and resins, conductive metals such as gold or silver, and thick film materials. PCB fabricators adopt via-filled design PCBs in order to meet customer demands for greater interconnect density and efficiency. They require via-filling processes that minimize voiding and surface residue, and ensure 100% filling of the via. For high-volume production, throughput and automation must also be increased. Mass imaging with enclosed-head screen printing can meet these criteria, with conductive via-filling performed successfully at aspect ratios of up to 8:1.

2.2.3 Additive process – the advantage for fine circuitry manufacturing
Currently, manufacturers are producing 20-micron lines and spaces on polyimide films for volume production with traditional subtractive processes. On the other hand, both the semi-additive and full-additive process have been expanding applications for double-sided and multilayer PCBs. Nowadays, semiconductor device manufacturers are talking about 90 nanometer lines (0.09 micron) as their next-generation design rules, and there are fine trace generation processes and the microvia generation of PCBs, especially in the flexible circuits industry. The technical capabilities of some leading PCB manufacturers for high-density circuits are much higher than their traditional multilayer board and flexible circuit counterparts. They now produce 5-micron lines and space for four- to six-layer circuits with 20-micron diameter vias. They will establish volume production capabilities of 2-micron lines and spaces with 10-micron vias in the next few years. These manufacturers are mostly using an additive process to build high-density circuits. The technologies developed for the next generation of ultra high-density circuits can be divided into three groups: the subtractive process, semi-additive process, and full-additive process. Figure 5 illustrates the fine line capabilities by adoption of different processes.

Figure 5. Fine-line capabilities of different processes.
There is no question that the full additive process has much a higher capability to generate fine line traces with microvias than the traditional subtractive process. The semi-additive process could be the middle position between the technologies. The manufacturers have been developing multilayer capabilities, and making them more widely available.

2.2.4 Embedded Passives technology

2.2.5 Laser Trimming technology

The better performance and lower cost of multilayer boards have been driving the development of technologies of embedded components. For tolerances of +1% or better, embedded components must be trimmed. For laser trimming, testing correctly is the most important issue and major requirements for testing are speed and accuracy. Accuracy is required to meet +1% tolerances. For considerations of speed, lasers should able to trim at repetition rates in excess of 10kHz. Probing speed is also important as it affects the overall throughput and cost of ownership of the system. More importantly, probes must be designed such that they do not block the laser beam.

2.2.6 Buried Capacitance(TM) and Thin Laminates

Buried capacitance (BC) products have been in use in many high-speed applications such as in the construction of complex multilayer PCBs and in the designing of power distribution circuits. The principle features of thin laminate BC technology are high-frequency by-pass decoupling capacitance, very low by-pass loop inductance, and EMI shielding. These three features of BC laminates have allowed circuit designers to make significant advances in the speed and performance of electronic systems.

As the spacing between the copper planes decreases (thinner dielectrics), the self and mutual inductance to currents on the planes decreases and an overall reduction in the high-frequency impedance is achieved. The overall reduction in impedance can be directly converted into a decrease in power distribution voltage noise and reduced EMI in the higher-frequency bands from several hundred MHz up to several GHz. The optimization of proprietary dielectric resin and copper foil has resulted in laminates that are rugged enough to process through typical PCB inner-layer processing.

The BC family of products provides circuit designers with alternative levels of increasing electrical performance for their embedded distributive capacitance needs in PCB design and functionality.
2.3 Reliability testing

2.3.1 Testing Basics
High-speed layout, blind and buried vias, and other restrictions render traditional testing methods less effective. There are two newer types of bare-board testers for the testing methods: the flying probe and the vision test. Flying probes have up to eight simultaneous moving probes on the top and bottom, to test for opens, shorts and, in some cases, high-voltage and dielectric breakdowns. Using target fiducials for alignment accuracy on the PCB, the probes can hit targets of 0.005", although some flying probe manufacturers claim even smaller targets. A bare board can be accurately tested using a flying probe. A flying probe is great for prototypes when the in-circuit test bed-of-nails fixture is still being manufactured. Also, today all flying probes have vision and some incorporate JTAG (IEEE 1149.1). Single-sided probes can hit targets of <0.005" and can therefore test flip-chip interconnects.
A vision test has been used to check layer-by-layer artwork against CAD data. With blind vias produced by a CO₂ laser, irregular via openings are the usual defects. The vision machine – either a two-dimensional x-ray/laser or an automatic optical inspection (AOI) – looks for debris inside the vias. A vision test is used mainly as a quality test (fillet size, joint quality, component skew, etc.), but is also very useful for finding catastrophic faults such as backward parts (polarized capacitors and diodes) and wrong-value parts (such as SMT resistors of a correct size but an incorrect value).

2.3.2 Conductive Anodic Filament (CAF)
The continuing process of miniaturization in the electronics industry is threatened by CAF. IPC instituted a CAF test procedure at the end of 2003, but OEMs in the industry use their own test vehicles along with their own test conditions. To date, there is no standard for CAF testing.
The causes behind the formation of CAF include: the voltage gradient, the via to glass orientation, ionic impurities, the moisture content in the laminate, the effect of thermal exposure on CAF, the hole wall quality, and re-lamination. Ionic impurities, moisture, thermal exposure, and re-lamination cycles affect the insulation resistance between the holes in the double-sided test vehicle that was studied. The drop in insulation resistance is a function of the hole wall-to-wall space. The 7 mil wall-to-wall space shows a larger drop in insulation resistance than the larger spaces (10, 15, and 20 mils) at any point in time.
Unless the industry develops PCB dielectric substrates that will be CAF resistant at these feature sizes, miniaturization could slow considerably. Fabricators will be
required to lower surface ionic impurities and develop better via formation techniques that will create minimum stress at the glass to resin interface over the hole wall. CAF should not form between layers as long as all of the other factors that affect the formation of CAF are controlled. A non-destructive way of finding CAF failures is optical transmission microscopy. Another way for finding CAF is by measuring the insulation resistance. It is well known in the industry that for CAF to occur within a laminate, certain conditions need to be in place. These include high humidity, high bias voltage under testing, high moisture content, surface and resin ionic impurities, glass-to-resin bond weakness, and exposure to high assembly temperatures (lead-free applications). There are four known ways that CAF forms at the surface and within the laminate: 1) hole-to-hole, 2) hole-to-trace, 3) trace-to-trace, and 4) layer-to-layer.

![Image](image_url)

Figure 6. Ion migration evaluation system
(Source: PCB Technology Centre, The Hong Kong Polytechnic University)

The ion migration evaluation system as shown in Figure 6 systemizes the environmental test chamber and measurement/evaluation system. It offers continuous, accurate, and effective ways of collecting insulation resistance data by applying stress voltage over specimens under specific temperature and humidity conditions. It detects changes in insulation resistance with high precision and excels in the detection of leak current. CAF can be easily caught by the system.

**Summary**

Compared to year 2003, the major PCB technologies keep moving forward in many different areas in 2004 as discussed. In PCB materials, the main foci are still high speed/frequency and lead-free materials. The design and manufacturing processes have also been improved in order to meet the ever-increasing demands of PCB requirements. The electronic miniaturization drives the development of new reliability tests and standards.
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